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10/044,185	01/09/2002	David B. Kramer	KRAMER 2-1-3	9779

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EXAMINER
MATTIS, JASON E

ART UNIT	PAPER NUMBER
2616	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/1/08*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☐ All   b)☐ Some *   c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
   Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

1.   This Office Action is in response to the Amendment filed 2/1/08. Claims 1-20 are

currently pending in the application.

Claim Rejections - 35 USC § 103

2.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

3.   Claims 1-3, 6-10, 13, and 14 rejected under 35 U.S.C. 103(a) as being

unpatentable over Reches (U.S. Publication US 2002/0110086 A1) in view of Dell et al.

(U.S. Publication US 2002/0085578 A1).

With respect to claims 1 and 8, Reches discloses a non-blocking crossbar and

method of operation **(See page 2 paragraph 24 of Reches for reference to a**

crossbar switch and a method for controlling the crossbar switch such that

packets are not blocked by each other). Reches also discloses n inputs and n

outputs **(See page 4 paragraphs 51-52 and Figure 1 of Reches for reference to the**

switch comprising N input ports and N output ports). Reches further discloses

each of the outputs having a destination FIFO and n crossbar FIFOs interposing

corresponding ones of the n inputs and the destination FIFO **(See page 4 paragraph**

52, page 4 paragraph 55, and Figure 1 of Reches for reference to each output port

having at least one output queue, which is an output FIFO, and for reference to

input ports maintaining an output queue for each possible output port, meaning

for each output port there are N queues corresponding to each of the N inputs

and interposed between corresponding ones of the N inputs and the destination

FIFOs). Reches also discloses a scheduler configured to cause a plurality of packets

that are unencapsulated, unsegmented, and of differing lengths to be transmitted from

one of the inputs toward one of the outputs when both the destination FIFO and an

interposing one of the crossbar FIFOs have sufficient memory to contain an entirety of a

packet of the plurality of packets **(See page 1 paragraph 8, page 4 paragraph 56 to**

page 5 paragraph 59, and Figure 1 of Reches for reference to forwarding variable

length packets that are not segmented or encapsulated and for reference to a

scheduler 40 that causes packets to be sent from an input to an output only when

it is determined that there is sufficient memory and resources to send the entire

packet in a set of time slots where the packet will not be blocked by other packets

currently being sent). Reches does not specifically disclose causing packets to be

transmitted only when a destination FIFO and an interposing one of the crossbar FIFOs

have sufficient memory at the same time to receive and then contain an entirety of the

packets.

   With respect to claims 1 and 8, Dell et al., in the field of communications,

discloses scheduling packets to be transmitted through a non-blocking crossbar only

when a destination FIFO and an interposing crossbar FIFO have sufficient memory at

the same time to receive and then contain an entirety of the packets **(See pages 8-9**

paragraphs 111-120, pages 9-10 paragraphs 128-137, and Figures 12 and 15-16 of Dell et al. for reference to input devices receiving grants to transmit cells only when there is no back-pressure in corresponding FIFO queues that make up a path from an input to the destination meaning that a cell is transmitted toward the output only when all queues have enough memory to contain the cell at the same time). Scheduling packets to be only when a destination FIFO and an interposing crossbar FIFO have sufficient memory at the same time to receive and then contain an entirety of the packets has the advantage of allowing packets to be more smoothly transmitted from an input through all intervening FIFOs to an output to prevent blocking at caused by congestion at any intervening FIFO.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Dell et al., to combine scheduling packets to be only when a destination FIFO and an interposing crossbar FIFO have sufficient memory at the same time to receive and then contain an entirety of the packets, as suggested by Dell et al., with the system and method of Reches, with the motivation being to allow packets to be more smoothly transmitted from an input through all intervening FIFOs to an output to prevent blocking at caused by congestion at any intervening FIFO.

With respect to claims 2 and 9, Reches discloses that the scheduler is further configured to select one of the inputs based upon a priority thereof **(See page 2 paragraph 18 of Reches for reference to forwarding packets from selected source ports based on priority level of the source port)**.

With respect to claims 3 and 10, Reches discloses that the scheduler is further configured to select one of the outputs based upon a priority thereof **(See page 4 paragraph 52 for reference to scheduler 40 forwarding packets to output ports based on output port queue priority levels)**.

With respect to claims 6 and 13, Reches discloses each output comprising an output arbiter configured to select one of the crossbar FIFOs and transfer a packet therein to the destination FIFO **(See page 4 paragraph 52 and page 5 paragraph 58 for reference to each output port having an arbiter that uses an arbitration scheme to transfer packets from input queues to output queues)**.

With respect to claims 7 and 14, Reches discloses that the arbiter is further configured to select one of the crossbar FIFOs based upon packet priority **(See page 3 paragraph 36 of Reches for reference to selecting packets to be transferred from input queues to output queues based on the priority of the packet)**.

4.   Claims 4, 5, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reches in view of Dell et al. and in further view of Chen et al. (U.S. Pat. 6975638 B1).

With respect to claims 4, 5, 11, and 12, the combination of Reches and Dell et al. does not specifically disclose that at least two of the n inputs are coupled to different types of packet based fabrics with the inputs and outputs being connected to a SONET network and two Ethernet networks.

With respect to claims 4, 5, 11, and 12, Chen et al. discloses a crossbar switch with inputs connected to Gigabit Ethernet networks and a SONET network **(See column 5 lines 7-18 and Figure 3 of Chen et al. for reference to a crossbar switching having inputs connected to Gigabit Ethernet networks and a SONET network)**. A crossbar switch with inputs connected to Gigabit Ethernet networks and a SONET network has the advantage of allowing the switch to transfer packet from both SONET and Ethernet network, which are highly used packet protocol networks.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Chen et al., to combine a crossbar switch with inputs connected to Gigabit Ethernet networks and a SONET network, as suggested by Chen et al., with the system and method of Reches and Dell et al., with the motivation being to allow the switch to transfer packet from both SONET and Ethernet network, which are highly used packet protocol networks.

5.   Claims 15-17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reches in view of Dell et al. and in further view of Hartmann et al. (U.S. Pat. 5905873).

With respect to claim 15, Reches discloses a multi-channel network line card for packet based networks **(See page 4 paragraphs 51-52 and Figure 1 of Reches for reference to a switch having input ports that correspond to a line multi-channel network line card)**. Reches also discloses n physical interfaces and inputs numbering at least three **(See page 4 paragraphs 51-52 and Figure 1 of Reches for reference**

to the switch comprising N input ports, which are physical interfaces, numbering

at least three). Reches further discloses a non-blocking crossbar coupled to the

physical interfaces **(See page 4 paragraphs 51-52 and Figure 1 of Reches for**

reference to a configurable switch unit 50, which corresponds to a non-blocking

crossbar coupled to the input ports). Reches also discloses n outputs that transmit

the packet to corresponding ones of the n physical interfaces **(See page 4 paragraphs**

51-52 and Figure 1 of Reches for reference to the switch comprising N output

ports transmitting packets to physical interfaces). Reches further discloses each of

the outputs having a destination FIFO and n crossbar FIFOs interposing corresponding

ones of the n inputs and the destination FIFO **(See page 4 paragraph 52, page 4**

paragraph 55, and Figure 1 of Reches for reference to each output port having at

least one output queue, which is an output FIFO, and for reference to input ports

maintaining an output queue for each possible output port, meaning for each

output port there are N queues corresponding to each of the N inputs and

interposed between corresponding ones of the N inputs and the destination

FIFOs). Reches also discloses a scheduler configured to cause a plurality of packets

that are unencapsulated, unsegmented, and of differing lengths to be transmitted from

one of the inputs toward one of the outputs when both the destination FIFO and an

interposing one of the crossbar FIFOs have sufficient memory to contain an entirety of a

packet of the plurality of packets **(See page 1 paragraph 8, page 4 paragraph 56 to**

page 5 paragraph 59, and Figure 1 of Reches for reference to forwarding variable

length packets that are not segmented or encapsulated and for reference to a

scheduler 40 that causes packets to be sent from an input to an output only when it is determined that there is sufficient memory and resources to send the entire packet in a set of time slots where the packet will not be blocked by other packets currently being sent). Reches does not specifically disclose causing packets to be transmitted only when a destination FIFO and an interposing one of the crossbar FIFOs have sufficient memory at the same time to receive and then contain an entirety of the packets. Reches also does not specifically disclose n network processors that convert a packet between protocols coupled to corresponding ones of the n physical interfaces.

With respect to claim 15, Dell et al., in the field of communications, discloses scheduling packets to be transmitted through a non-blocking crossbar only when a destination FIFO and an interposing crossbar FIFO have sufficient memory at the same time to receive and then contain an entirety of the packets **(See pages 8-9 paragraphs 111-120, pages 9-10 paragraphs 128-137, and Figures 12 and 15-16 of Dell et al. for reference to input devices receiving grants to transmit cells only when there is no back-pressure in corresponding FIFO queues that make up a path from an input to the destination meaning that a cell is transmitted toward the output only when all queues have enough memory to contain the cell at the same time)**. Scheduling packets to be only when a destination FIFO and an interposing crossbar FIFO have sufficient memory at the same time to receive and then contain an entirety of the packets has the advantage of allowing packets to be more smoothly transmitted from an input through all intervening FIFOs to an output to prevent blocking at caused by congestion at any intervening FIFO.

It would have been obvious for one of ordinary skill in the art at the time of the

invention, when presented with the work of Dell et al., to combine scheduling packets to

be only when a destination FIFO and an interposing crossbar FIFO have sufficient

memory at the same time to receive and then contain an entirety of the packets, as

suggested by Dell et al., with the system and method of Reches, with the motivation

being to allow packets to be more smoothly transmitted from an input through all

intervening FIFOs to an output to prevent blocking at caused by congestion at any

intervening FIFO.

With respect to claim 16, Reches discloses a fast pattern processor that

receives a packet from a physical interface and analyzes and classifies the packet **(See**

page 3 paragraph 36 of Reches for reference to an input port receiving a packet

and analyzing the packet to determine parameters including the priority of the

packet, which is a classification of the packet). Reches does not disclose

processing the packet and converting the packet into an appropriate network protocol.

With respect to claims 15 and 16, Hartmann et al., in the field of

communications, discloses network processors coupled to corresponding physical

interfaces that convert received packets between protocols **(See the abstract of**

Hartmann et al. for reference to port adaptors, which are network processors,

coupled to input ports, which are physical interfaces, that receive packets and

convert them between different types of communication formats, which are

protocols). Using network processors coupled to corresponding physical interfaces

that convert received packets between protocols has the advantage of allowing all

packets being sent through a crossbar switch to have a common protocol, such that it is easier to switch the packets **(See the abstract of Hartmann et al. for reference to this advantage)**.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Hartmann et al., to combine using network processors coupled to corresponding physical interfaces that convert received packets between protocols, as suggested by Hartmann et al., with the system and method of Reches and Dell et al., with the motivation being to allow all packets being sent through a crossbar switch to have a common protocol, such that it is easier to switch the packets.

With respect to claim 17, Reches discloses that the scheduler is further configured to select one of the inputs based upon a priority thereof **(See page 2 paragraph 18 of Reches for reference to forwarding packets from selected source ports based on priority level of the source port). Reches also discloses that the scheduler is further configured to select one of the outputs based upon a priority thereof (See page 4 paragraph 52 for reference to scheduler 40 forwarding packets to output ports based on output port queue priority levels)**.

With respect to claim 20, Reches discloses each output comprising an output arbiter configured to select one of the crossbar FIFOs and transfer a packet therein to the destination FIFO **(See page 4 paragraph 52 and page 5 paragraph 58 for reference to each output port having an arbiter that uses an arbitration scheme to transfer packets from input queues to output queues)**. Reches discloses that the

arbiter is further configured to select one of the crossbar FIFOs based upon packet

priority **(See page 3 paragraph 36 of Reches for reference to selecting packets to**

be transferred from input queues to output queues based on the priority of the

packet).

6.   Claims 18 and 19 rejected under 35 U.S.C. 103(a) as being unpatentable over

Reches in view of Dell et al. and Hartmann et al. and in further view of Chen et al.

With respect to claims 18 and 19, the combination of Reches, Dell et al., and

Hartmann et al. does not specifically disclose that at least two of the n inputs are

coupled to different types of packet based networks with the inputs and outputs being

connected to a SONET network and two Ethernet networks.

With respect to claims 18 and 19, Chen et al. discloses a crossbar switch with

inputs connected to Gigabit Ethernet networks and a SONET network **(See column 5**

lines 7-18 and Figure 3 of Chen et al. for reference to a crossbar switching having

inputs connected to Gigabit Ethernet networks and a SONET network). A crossbar

switch with inputs connected to Gigabit Ethernet networks and a SONET network has

the advantage of allowing the switch to transfer packet from both SONET and Ethernet

network, which are highly used packet protocol networks.

It would have been obvious for one of ordinary skill in the art at the time of the invention,

when presented with the work of Chen et al., to combine a crossbar switch with inputs

connected to Gigabit Ethernet networks and a SONET network, as suggested by Chen

et al., with the system and method of Reches, Dell et al., and Hartmann et al., with the

motivation being to allow the switch to transfer packet from both SONET and Ethernet network, which are highly used packet protocol networks.

Response to Arguments

7.   Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8.   Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON E. MATTIS whose telephone number is (571)272-3154. The examiner can normally be reached on M-F 8AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Firmin Backer can be reached on (571)272-6703. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JEM

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